Cortex-A72 Microarchitecture

Pi 3 B+ Features

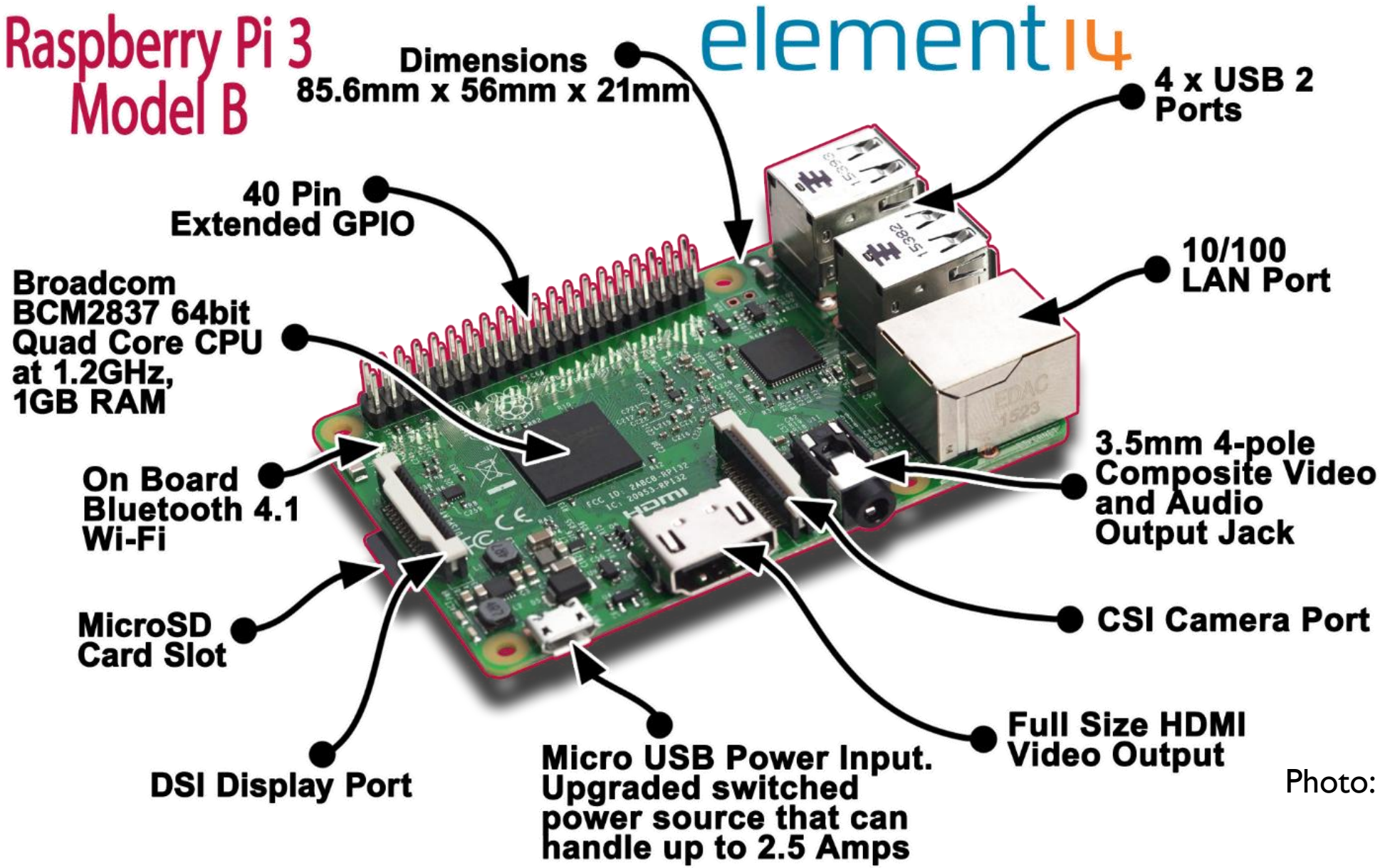


Photo: Element 14

Pi 4B Features

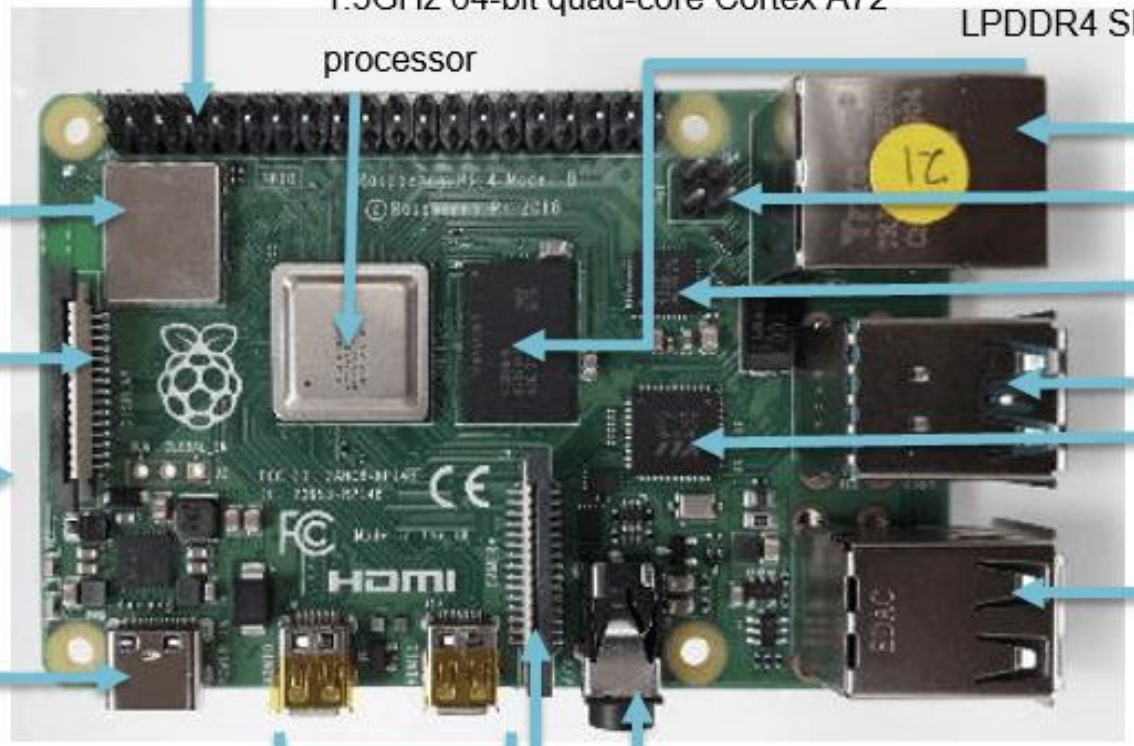
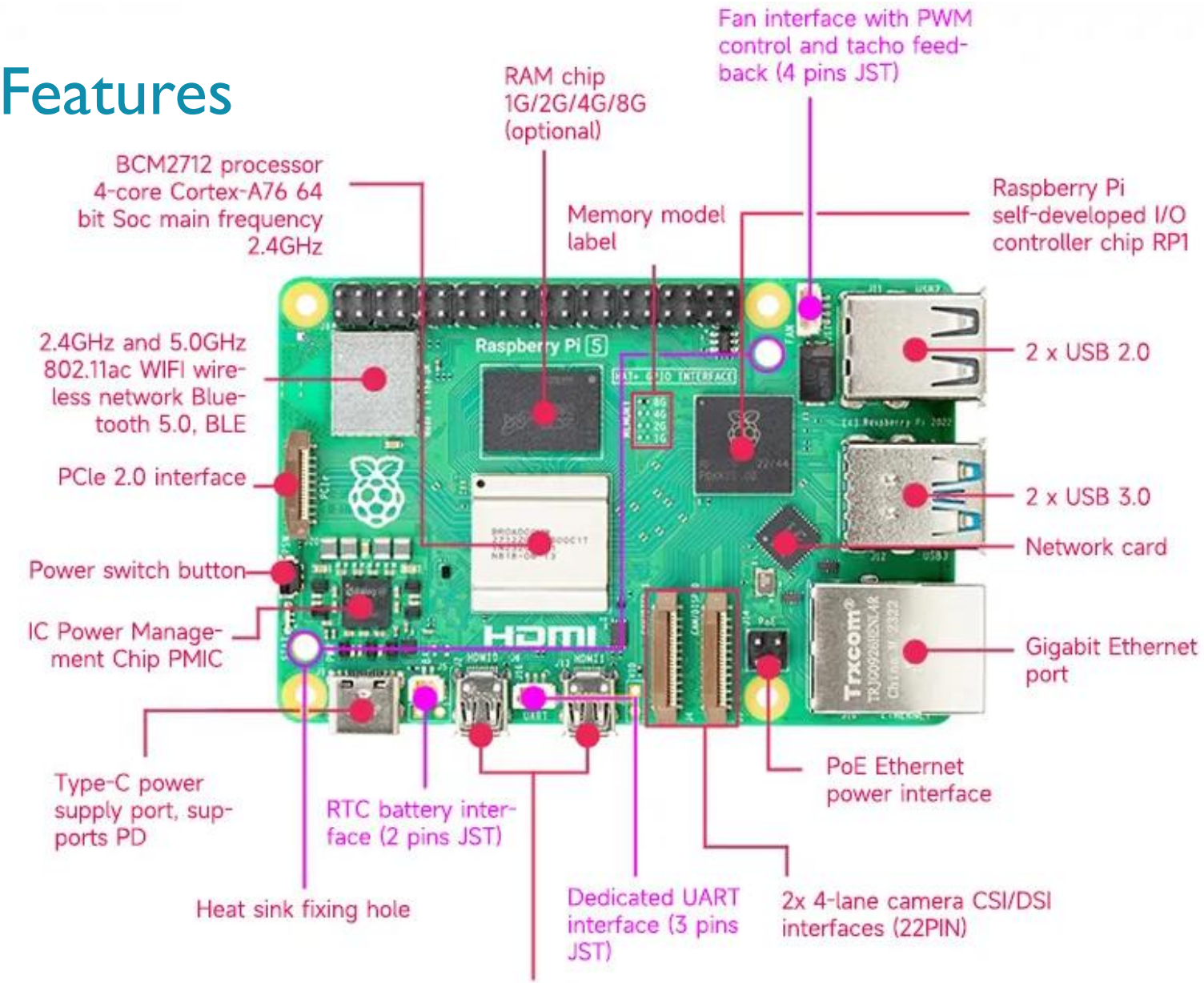


Photo: Premier Farnell

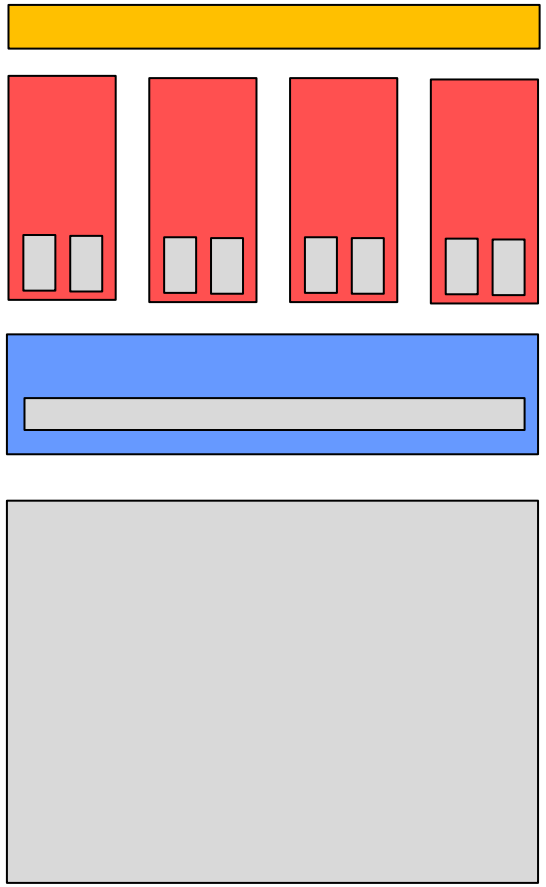
Pi 5B Features

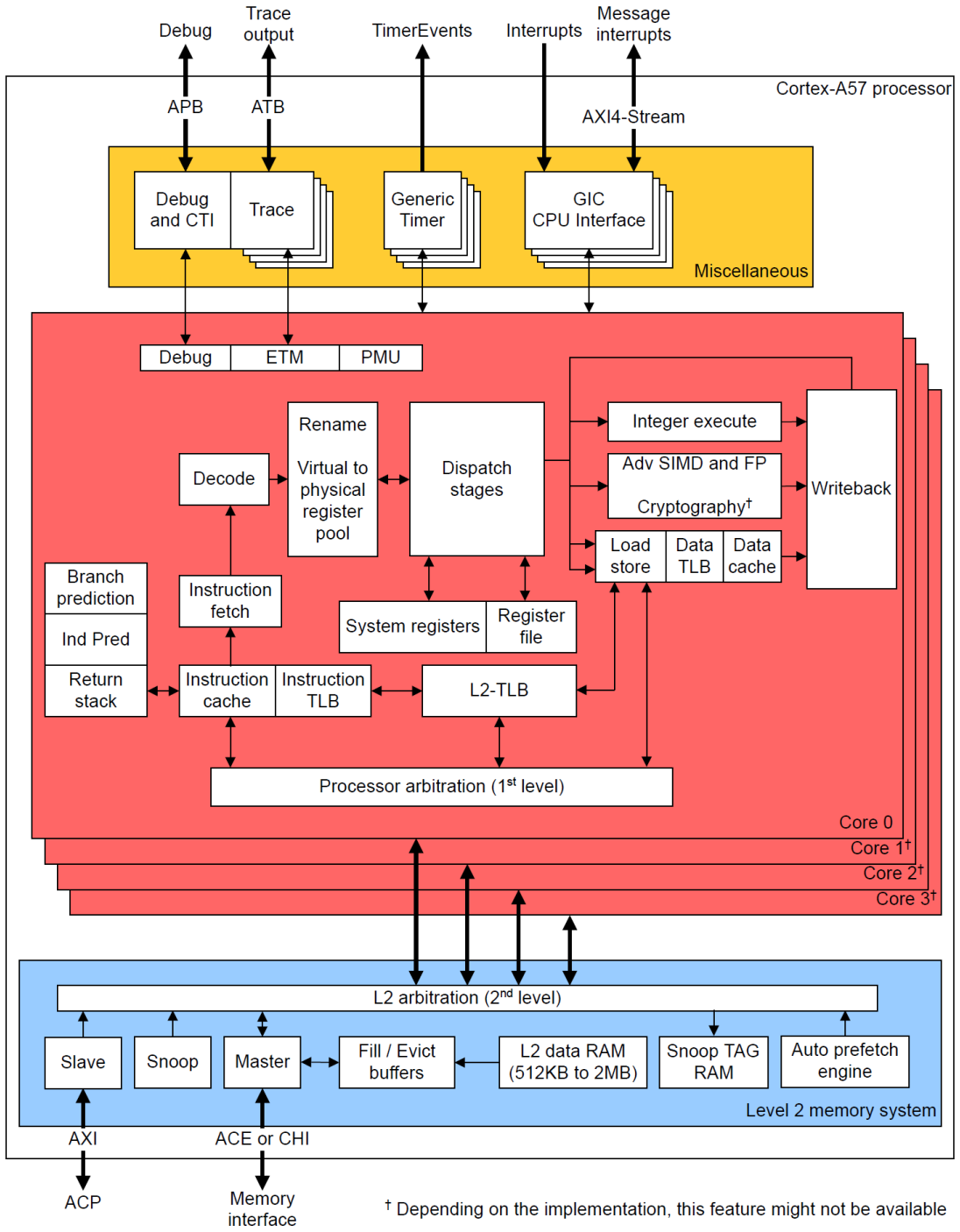


Raspberry Pi Processors and Performance

Board	SoC	CPU Freq	Processor (# Cores)	ARM ISA	GFLOPS	Video Coprocessor
5	BCM2712	2.4 GHz	Cortex-A76 (4)	V8	?	VideoCore VII (800 MHz)
4 B	BCM2711	1.5 GHz	Cortex-A72 (4)	V8	9.92 (1 GB), 13.5 (4 GB)	VideoCore VI (500 MHz)
3 B+	BCM2837B0	1.4 GHz	Cortex-A53 (4)	V7	5.3	VideoCore IV
3 B	BCM2837	1.2 GHz	Cortex-A53 (4)	V7	3.62	VideoCore IV
3 A+	BCM2837B0	1.4 GHz	Cortex-A53 (4)	V7		VideoCore IV
2 V1.2	BCM2837	1.2 GHz	Cortex A53 (4)	V7	4.43	VideoCore IV
Zero 2 W	RP3A0 / BCM2710A1	1 GHz	Cortex-A53 (4)	V7		VideoCore IV
2 V1.1	BCM2836	900 MHz	Cortex-A7 (4)	V7	1.47	
Zero W/WH	BCM2835	1 GHz	ARM1176JZF-S (1)	V6		VideoCore IV

Pi 3: Cortex-A57





Debug and trace, timers, interrupts

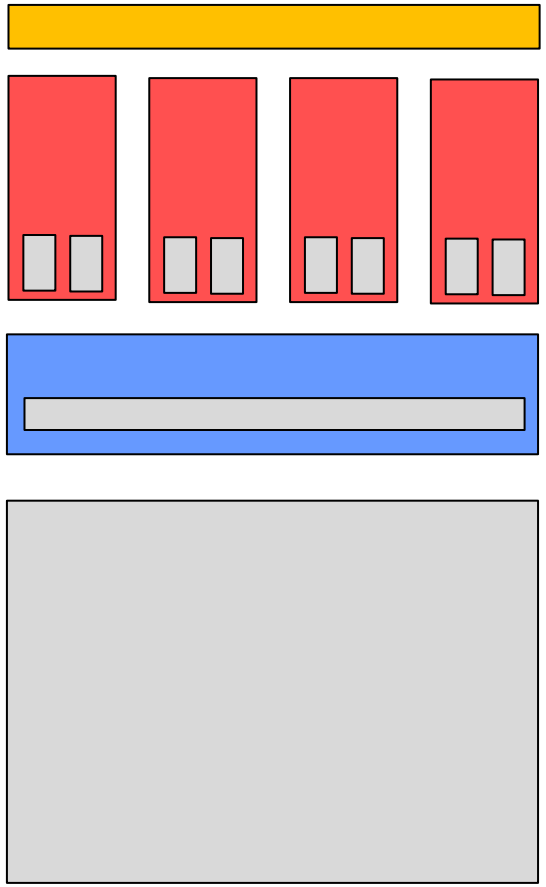
Four cores

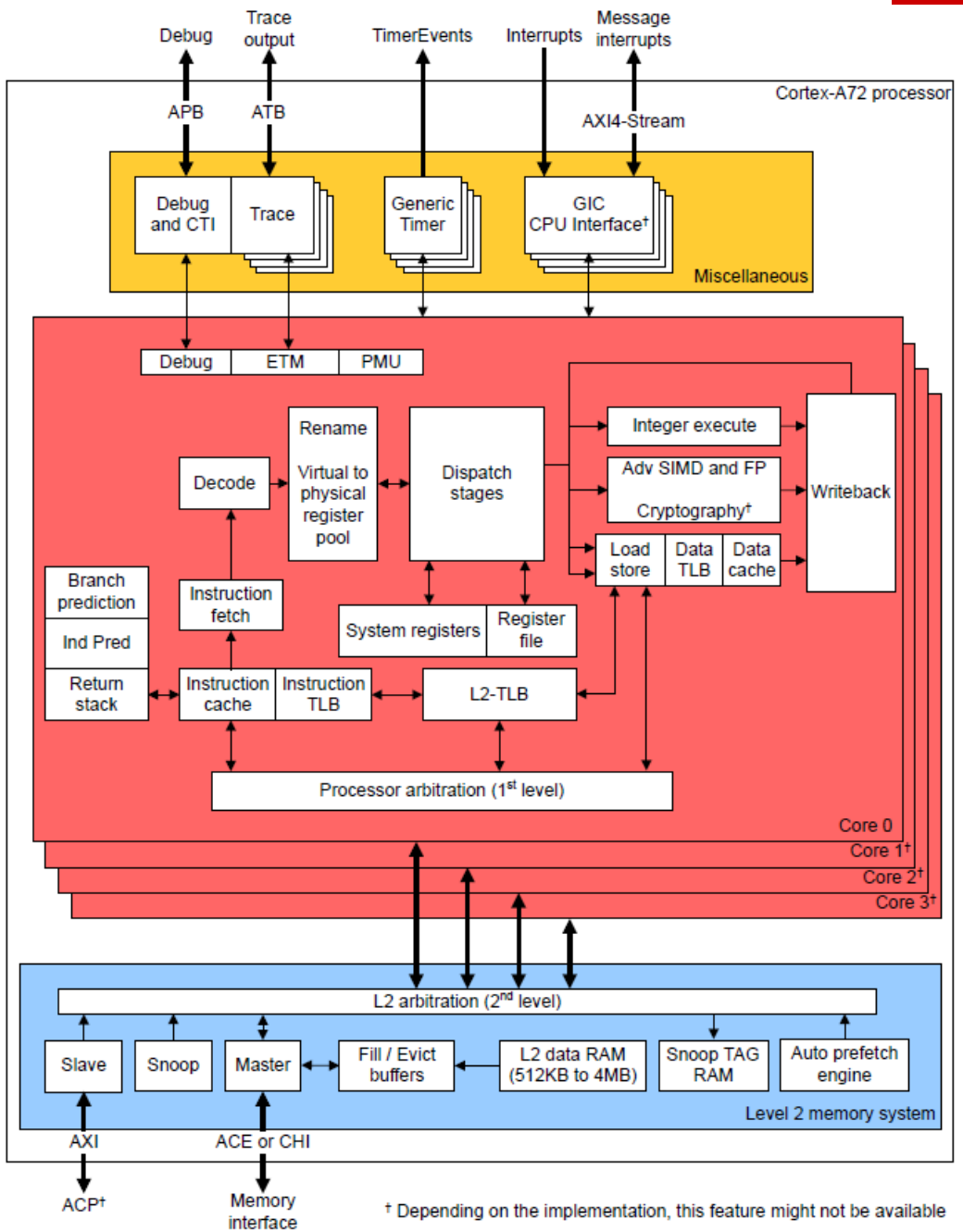
Each has Level 1 instruction and data caches

Level 2 memory system

Memory interface

Pi 4: Cortex-A72





Debug and trace, timers, interrupts

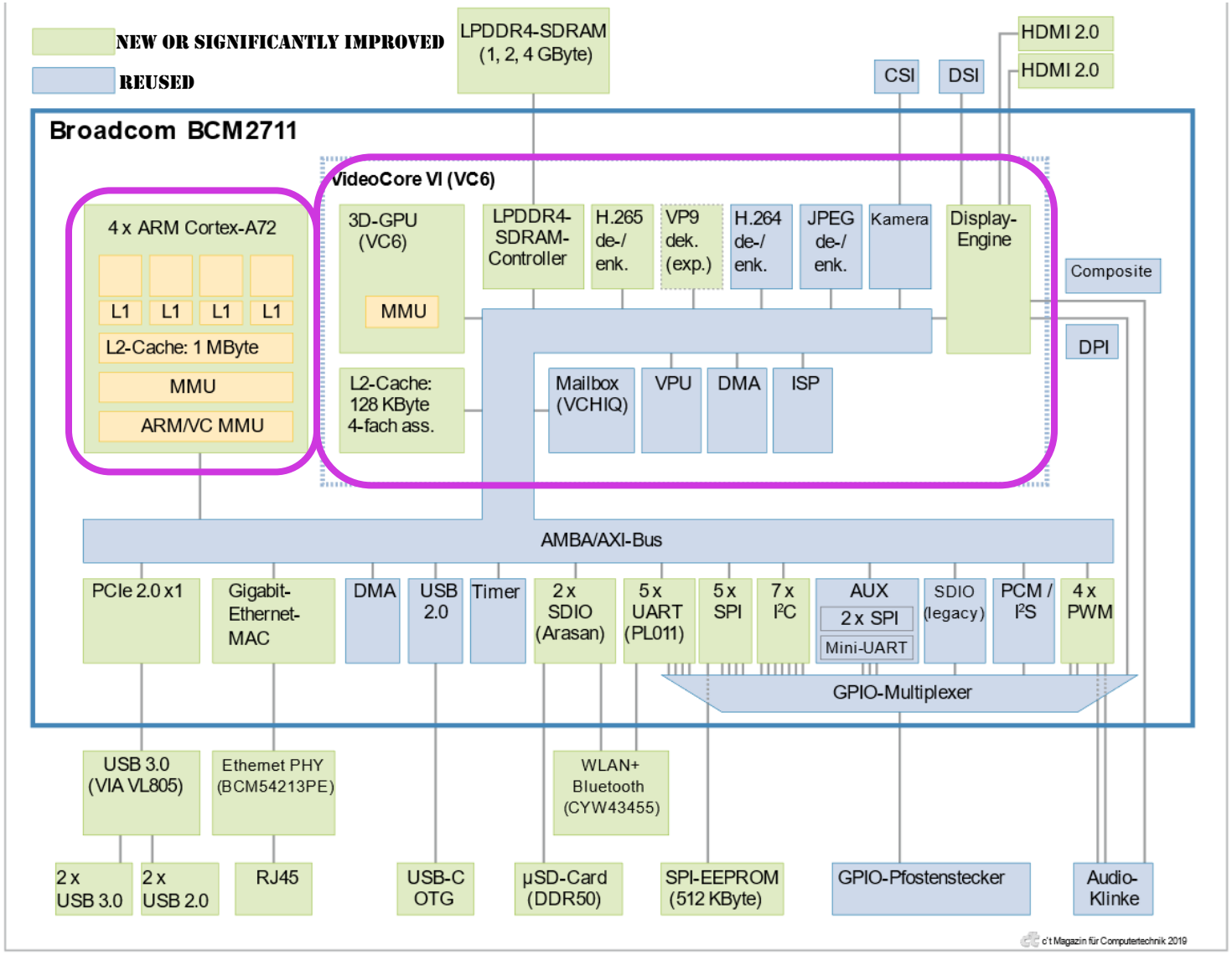
Four cores

- *Each has Level 1 instruction and data caches*

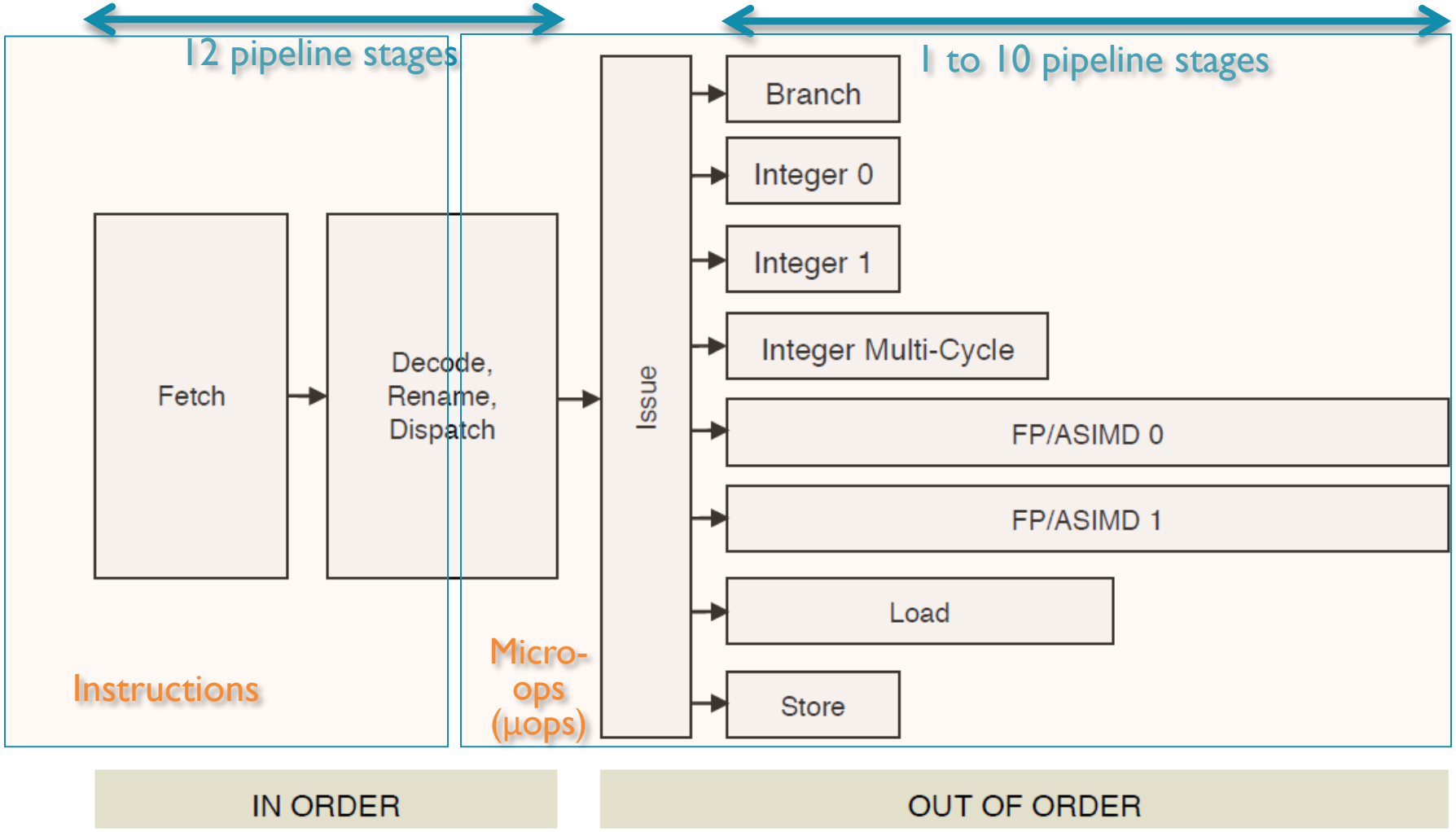
Level 2 memory system

Memory interface

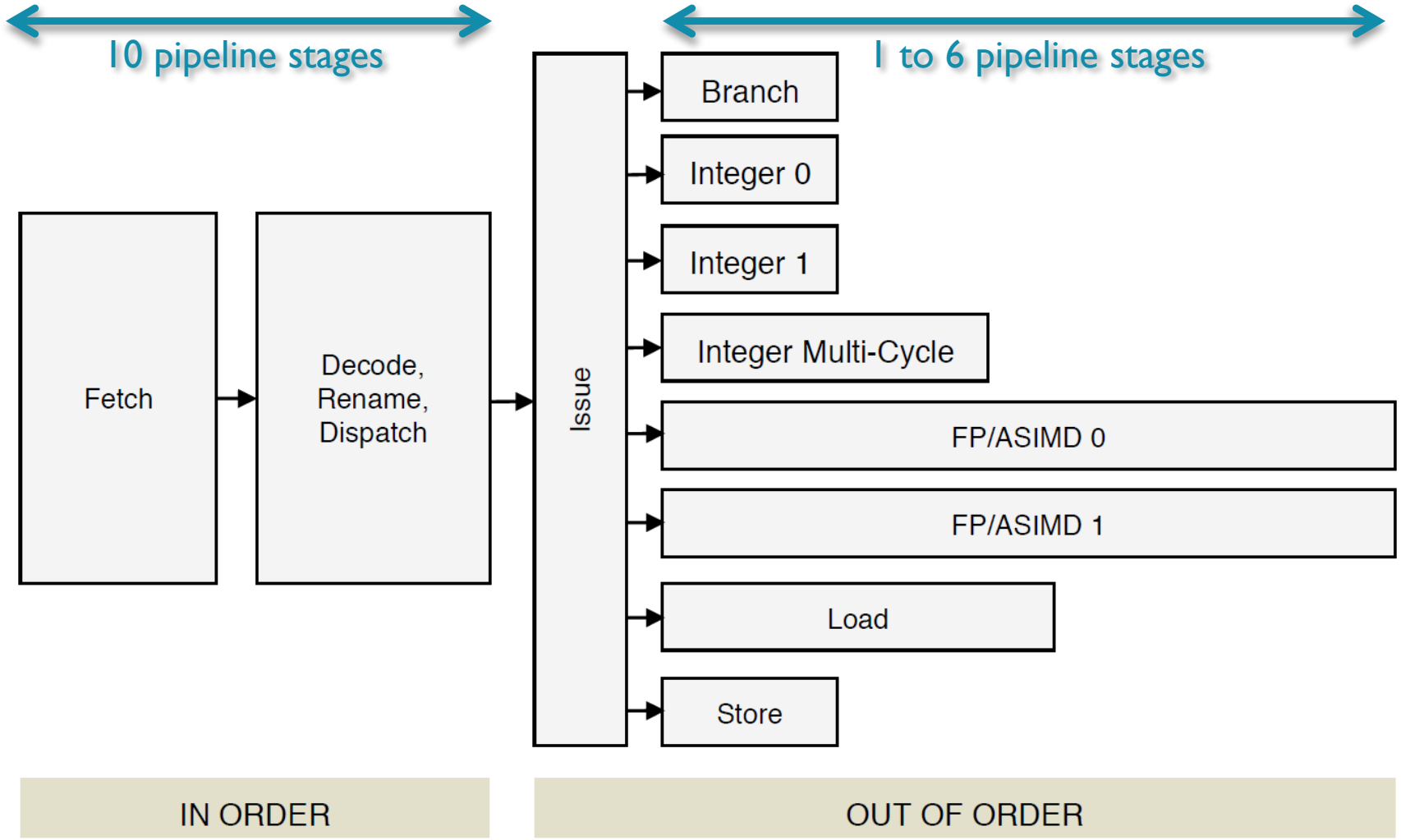
BCM2711


NEW OR SIGNIFICANTLY IMPROVED
REUSED
LPDDR4-SDRAM (1, 2, 4 GByte)
HDMI 2.0
HDMI 2.0
CSI
DSI
Broadcom BCM2711
VideoCore VI (VC6)
4 x ARM Cortex-A72
L1
L1
L1
L1
L2-Cache: 1 MByte
MMU
ARM/VC MMU
3D-GPU (VC6)
MMU
L2-Cache: 128 KByte 4-fach ass.
LPDDR4-SDRAM-Controller
H.265 de-/enk.
VP9 dek. (exp.)
H.264 de-/enk.
JPEG de-/enk.
Kamera
Display-Engine
Composite
DPI
Mailbox (VCHIQ)
VPU
DMA
ISP
AMBA/AXI-Bus
PCIe 2.0 x1
Gigabit-Ethernet-MAC
DMA
USB 2.0
Timer
2 x SDIO (Arasan)
5 x UART (PL011)
5 x SPI
7 x I²C
AUX
2 x SPI
Mini-UART
SDIO (legacy)
PCM / I²S
4 x PWM
GPIO-Multiplexer
USB 3.0 (VIA VL805)
Ethernet PHY (BCM54213PE)
WLAN+ Bluetooth (CYW43455)
2 x USB 3.0
2 x USB 2.0
RJ45
USB-C OTG
µSD-Card (DDR50)
SPI-EEPROM (512 KByte)
GPIO-Pfostenstecker
Audio-Klinke
c't Magazin für Computertechnik 2019

Cortex-A57 Instruction Pipeline

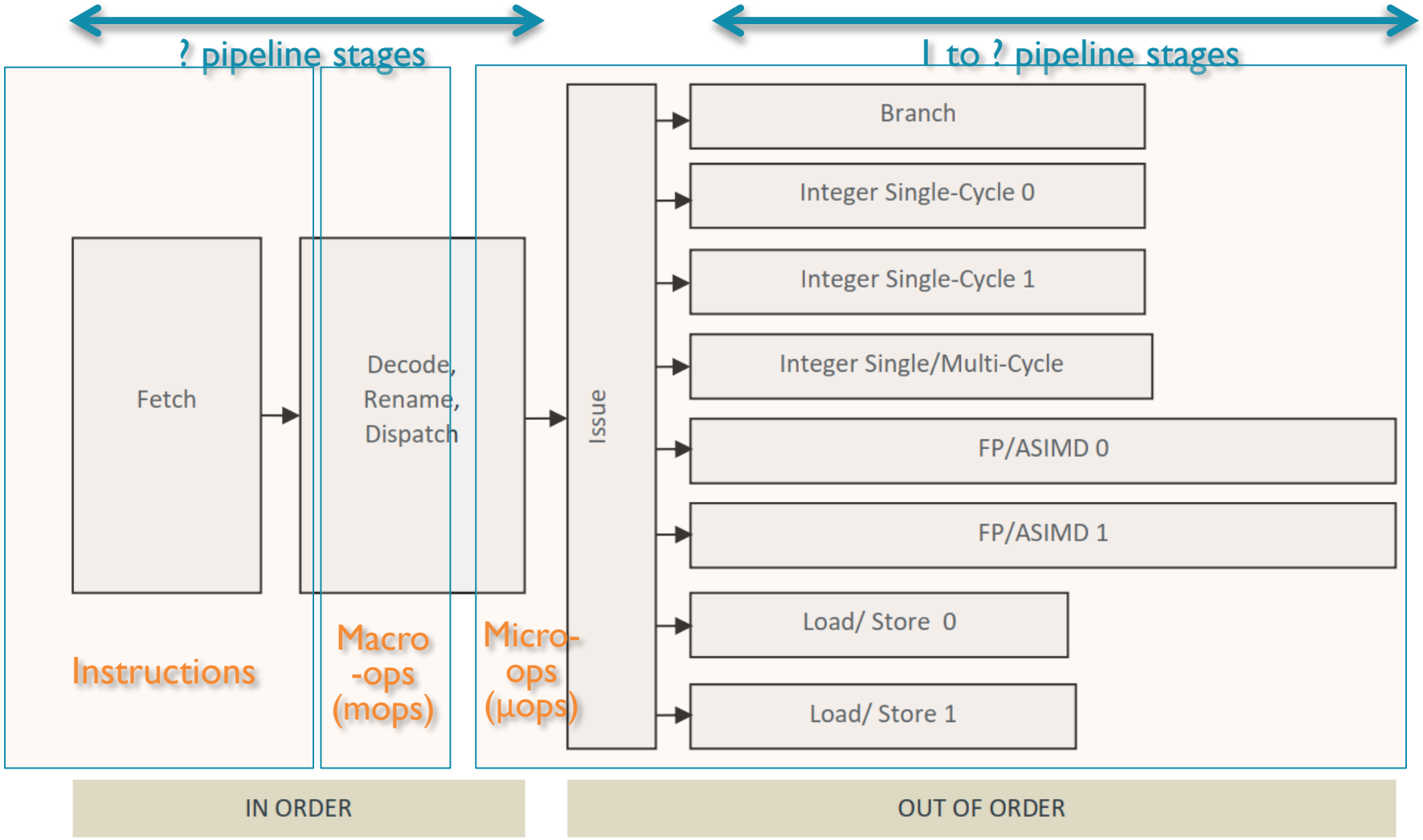


Cortex-A72 Instruction Processing Pipeline



New FP/ASIMD units are only 6 pipe stages long (vs. 10 on A57)

Cortex-A76 Instruction Processing Pipeline



ARM Cortex-A57 Block Diagram

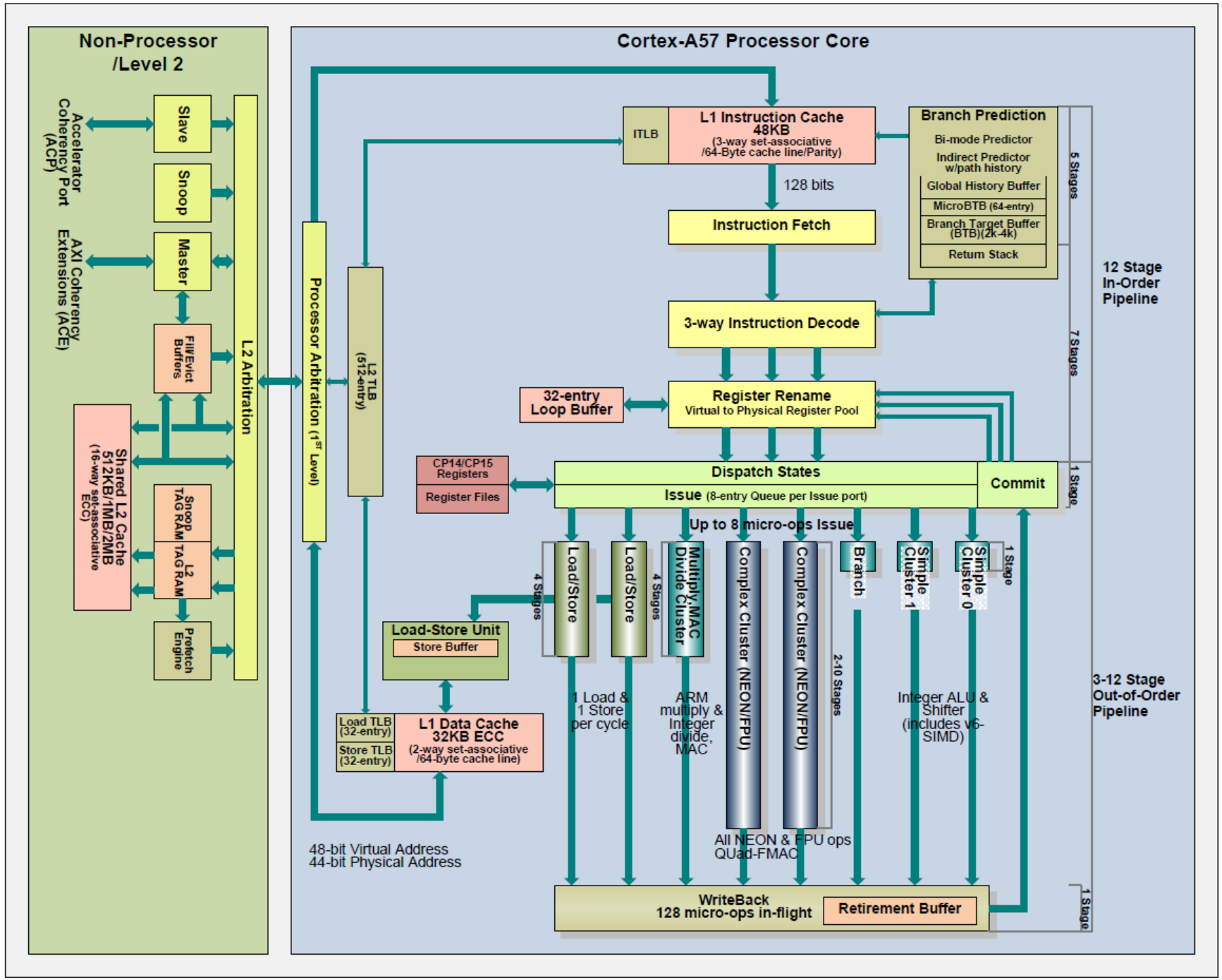


Diagram: Hiroshi Goto
PC Watch

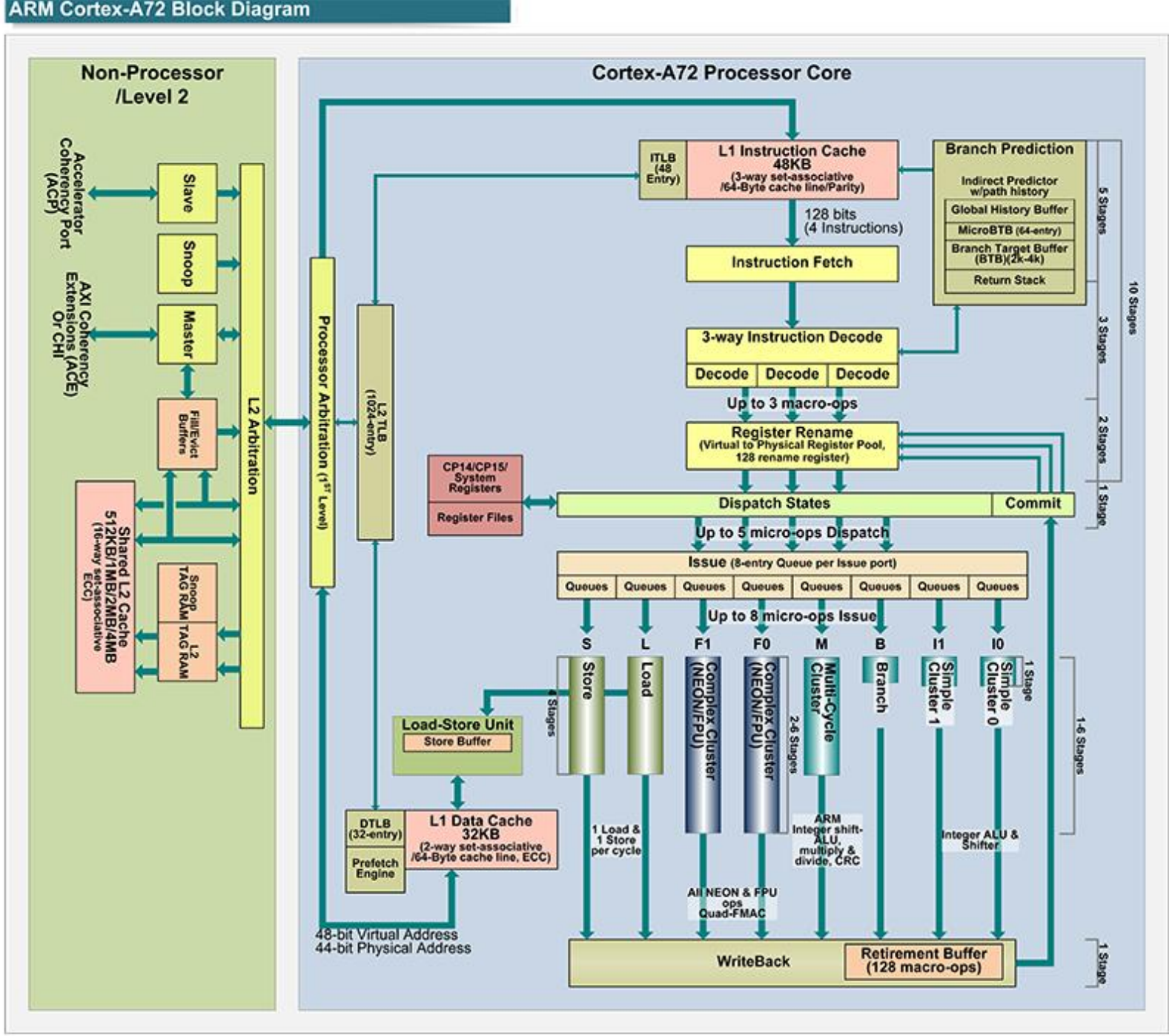
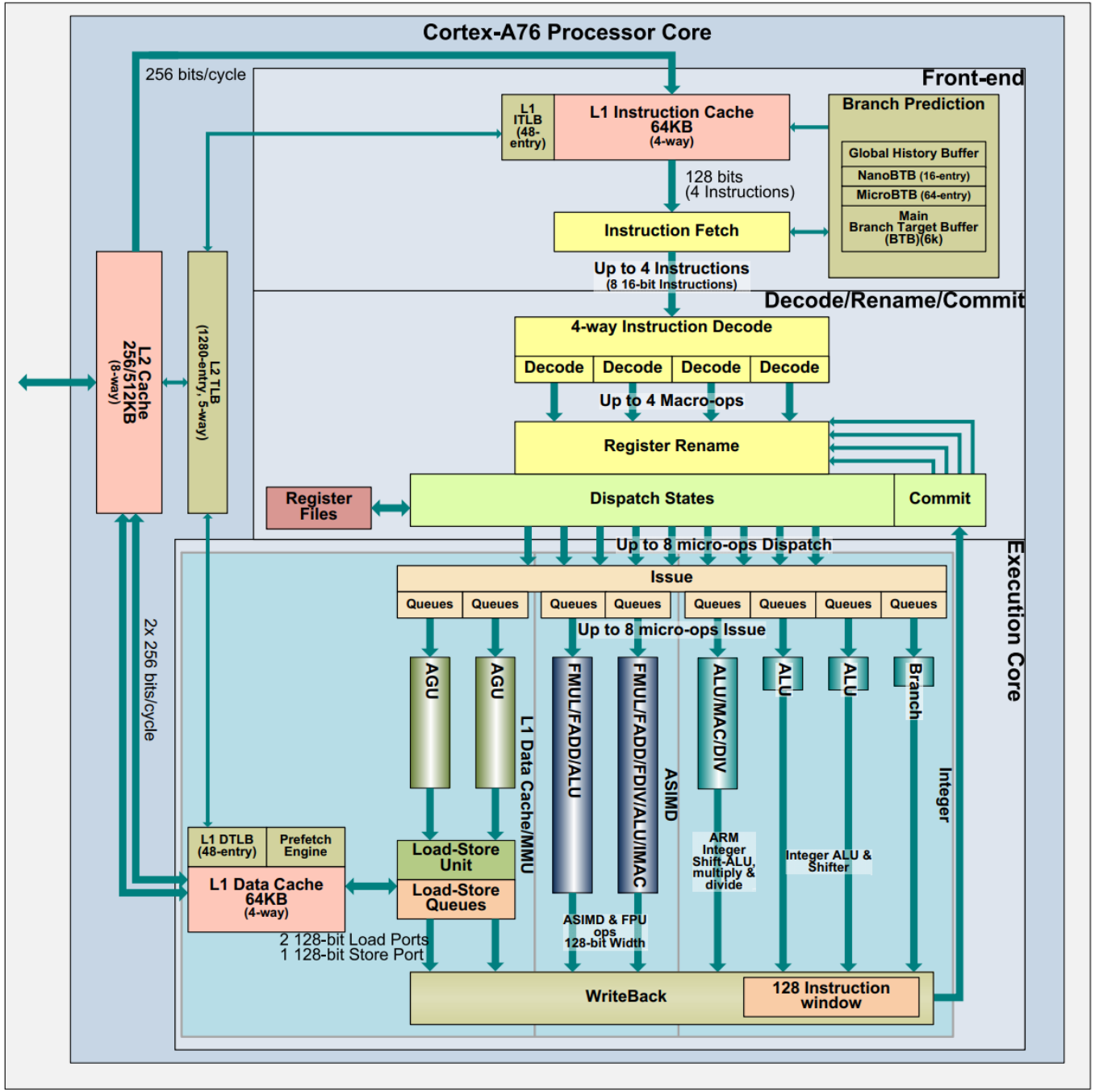


Diagram: Hiroshi Goto
PC Watch

ARM Cortex-A76 Block Diagram



Cortex-A57 Instruction Latencies

Integer Instruction Type	Result Latency
Branch	1-3
Arithmetic, Logic	1-2
Move, Shift	1-2
Divide	4-20, blocking
Multiply	3-5
Saturating and Parallel Arithmetic	2-5
Misc. Data Processing	1-4
Load	4-5
Store	1-3

Other Instruction Type	Result Latency
FP Data Processing	3-10
FP Divide	7-17 (SP), 7-32 (DP), blocking
FP Square Root	7-17 (SP), 7-32 (DP), blocking
FP Load	5
FP Store	1
ASIMD Integer	3-6
ASIMD FP	3-9
ASIMD Misc.	3-10
ASIMD Load	5-9
ASIMD Store	1-4
Crypto	3-6
CRC	3

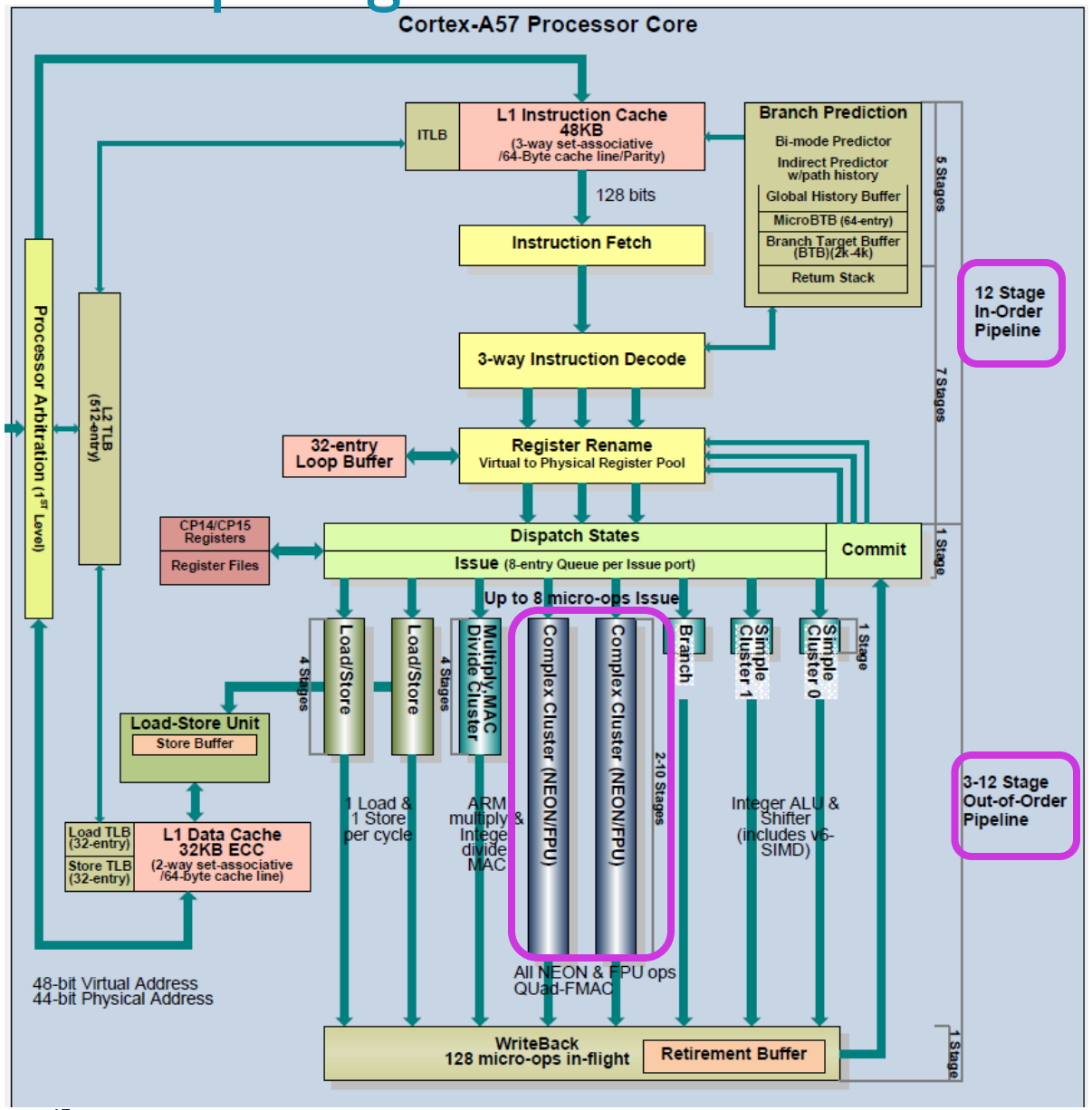
Cortex-A72 Instruction Latencies

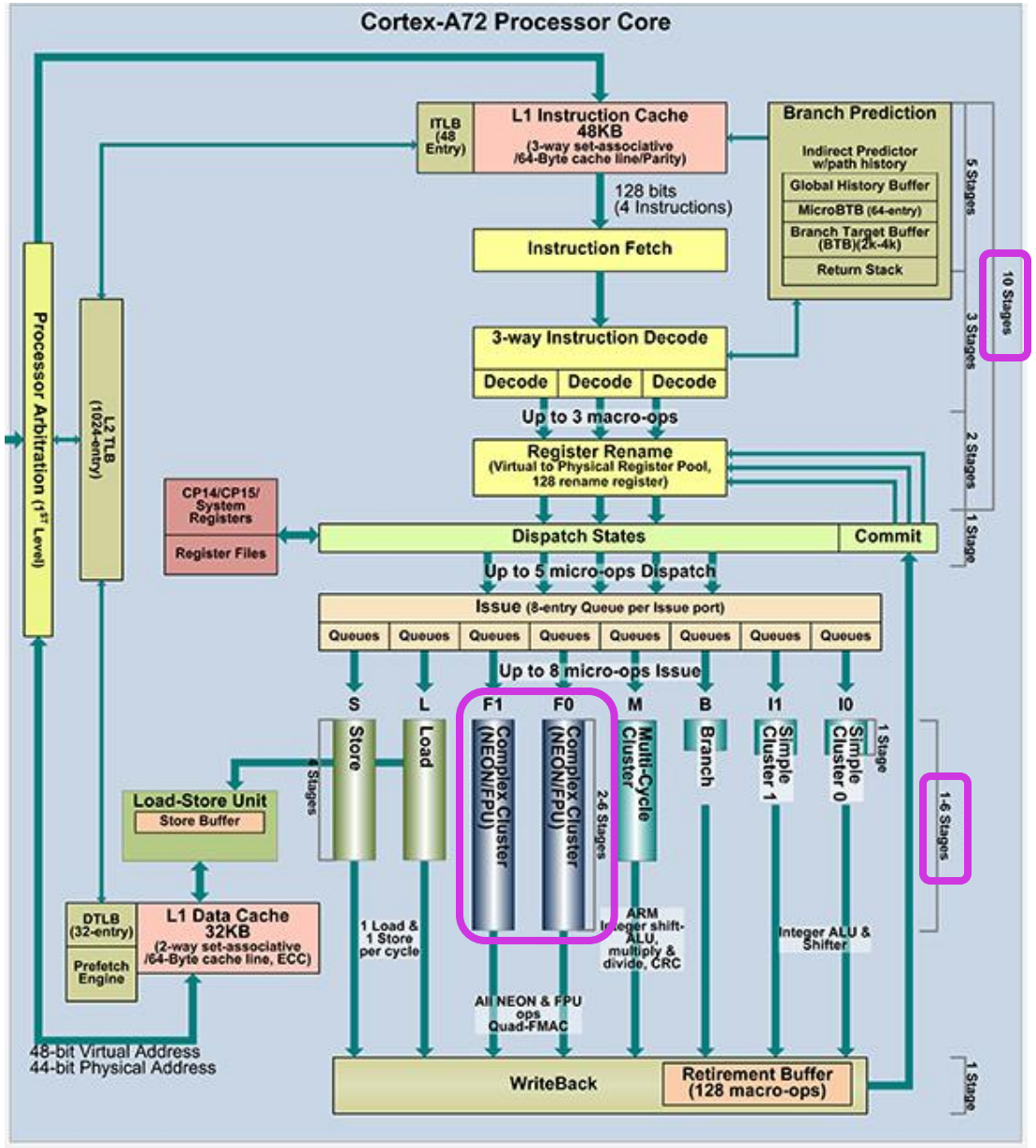
Integer Instruction Type	Result Latency
Branch	1
Arithmetic, Logic	1-2
Move, Shift	1-2
Divide	4-20. Blocking
Multiply	3-6
Saturating and Parallel Arithmetic	2-4
Misc. Data Processing	1-4
Load	4-5
Store	1-3

3 to 12 pipeline stages

Other Instruction Type	Result Latency
FP Data Processing	3-7
FP Divide	6-11 (SP), 6-18 (DP). Blocking
FP Square Root	6-17 (SP), 6-32 (DP). Blocking
FP Load	5-6
FP Store	1-4
ASIMD Integer	3-5
ASIMD FP	3-7
ASIMD Misc.	3-8
ASIMD Load	5-9
ASIMD Store	1-4
Crypto	3-6
CRC	2

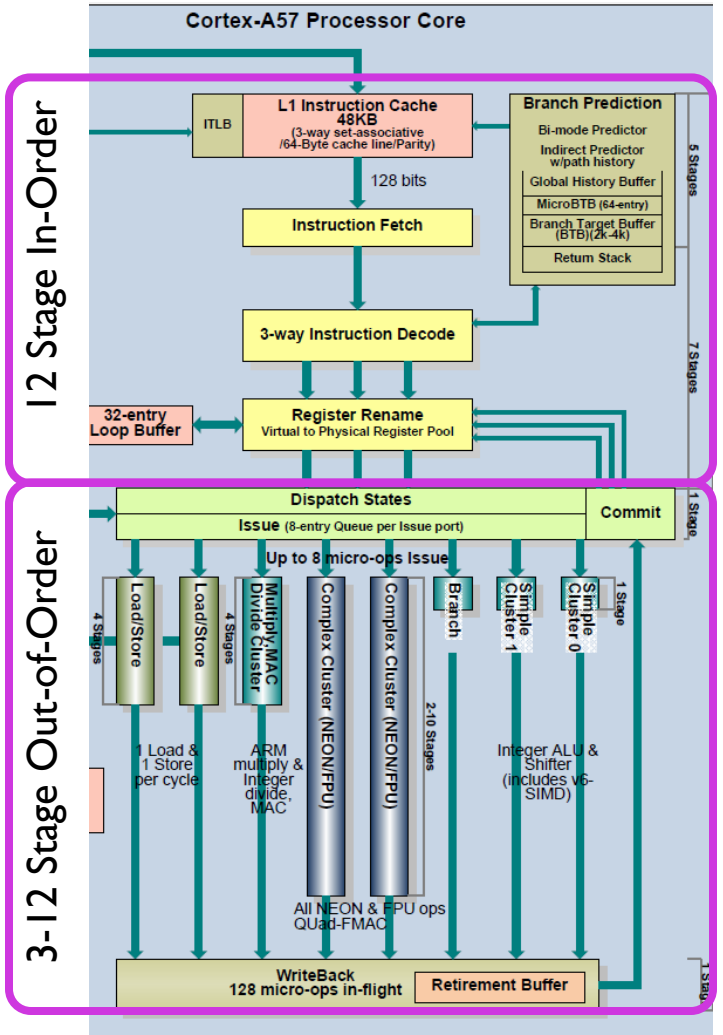
Comparing Cores: A57 and A72

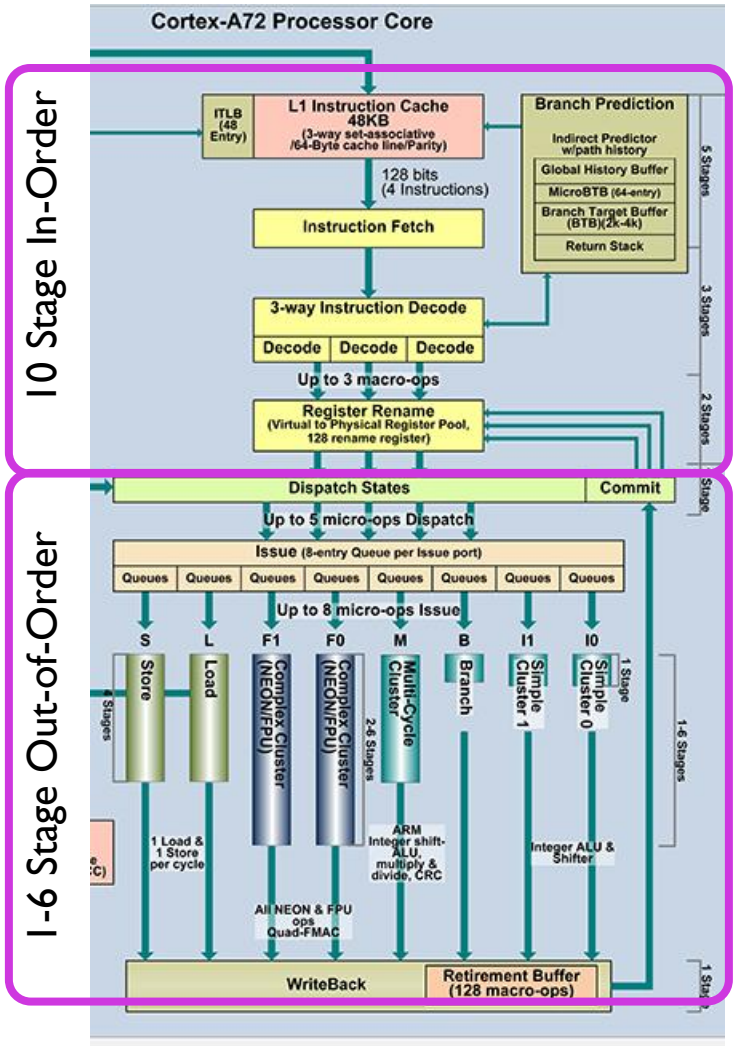


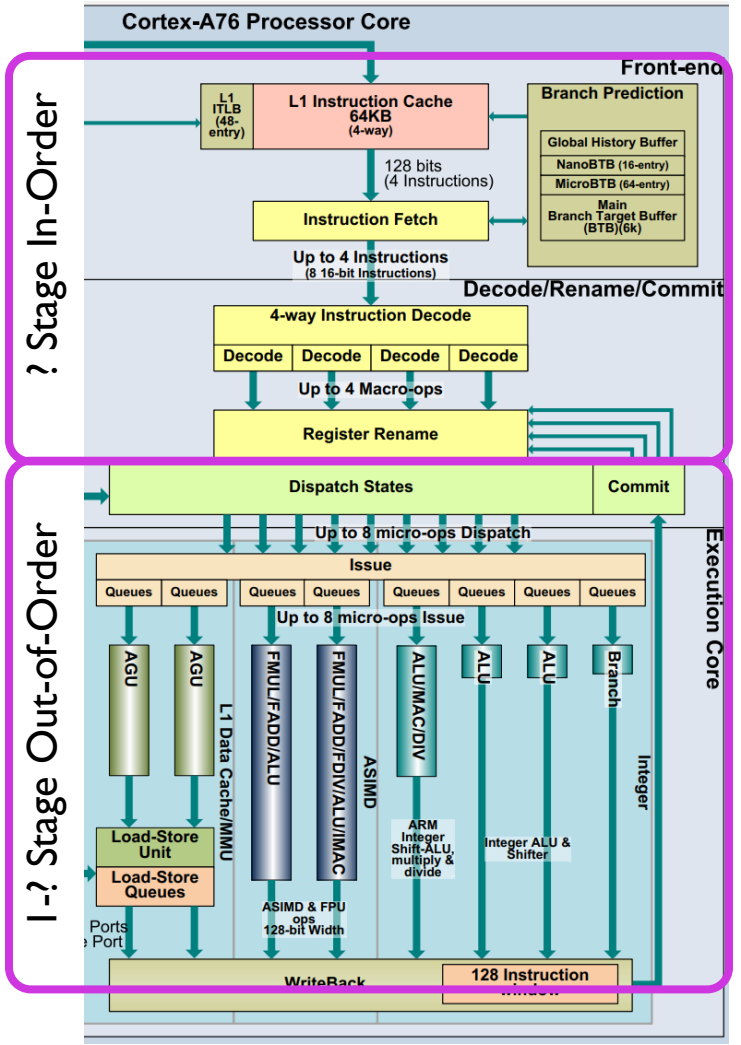


Diagrams: Hiroshi Goto, PC Watch

Comparing Cores: A57, A72, A76







Diagrams: Hiroshi Goto, PC Watch

Looking Forward: ARM CPU Core Comparison

	Cortex-A15	Cortex-A57 RPi 3	Cortex-A72 RPi 4	Cortex-A73	Cortex-A75	Cortex-A76 RPi 5	Cortex-A77	Cortex-A78
ARM ISA	ARMv7 (32-bit)	ARMv8 (32/64-bit)		ARMv8 (32/64-bit)				
Decoder Width	3 ops			2 ops	3 ops	4 ops	4 ops	4 ops
Maximum Pipeline Length	19 stages		16 stages					
Integer Pipeline Length	14 stages			11-12	11-13	11-13	11-13	?
Dispatch Width for Out of Order Execution	N/A (in-order)	3-wide	5-wide	4-wide	6-wide	8-wide	10-wide	?
DMIPS/MHz (Wikipedia)		4.6	4.72	6.35	8.2 - 9.5	10.7 - 12.4	?	?
Branch Units	1							
FP/NEON ALUs	2x64-bit	2x128-bit				2x128-bit		
L1 Cache	32KB I$ + 32KB D$	48KB I$ + 32KB D$				64KB I$ + 64KB D$		
L2 Cache	512KB - 4MB	512KB - 2MB	512KB - 4MB			512 KB		

Cortex-A76 Resources

- Arm
  - https://developer.arm.com/Processors/Cortex-A76
  - Arm® Cortex®-A76 Software Optimization Guide

- AnandTech: Arm's Cortex-A76 CPU Unveiled: Taking Aim at the Top for 7nm
  - Pipeline depth?
    - 13 stage implementation, latency of 11 stages due to overlap between branch predict path (2nd cycle) and fetch path (1st cycle)
    - Front-End Stages
      - Branch predict + Fetch: 2+2=4, effectively 3
      - Align and decode to macro-ops: 2
      - Rename and dispatch micro-ops: 1
    - Back-End Stages