

3/24/22

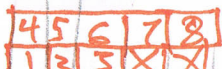
Why is RPi4 so much faster than FRDM-KL25Z?

- Clock speed. 1.8 GHz vs 48 MHz
- RAM size — Virtual Memory
speed — fast enough? 32 bits at 1.8 GHz
- Multicore — 4 cores
- (— Looser constraints)
- Graphics Processor
- Better Instructions
- Better μ Arch. (Implementation)



3/24/22

Multicore



- Cortex A72 - 4 cores

Superscalar



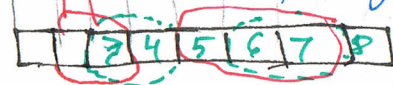
Better Instrs



Faster clock



Program



start

t (us)

end

- Changes ISA → Change program, compiler

Pipelining - 16 pipestages, 1.5 GHz vs 48 MHz

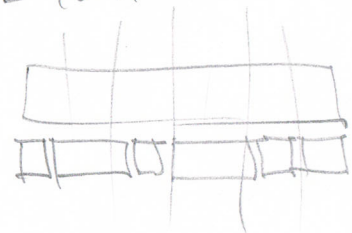
$$\frac{16}{2} = 8$$

160T
2 stage

$$\frac{1.5 \text{ GHz}}{48 \text{ MHz}} = \frac{1.5 \text{ GHz}}{0.05 \text{ GHz}} = 30$$

$$\frac{7}{48 \text{ MHz}} = \frac{1}{24 \text{ MHz}} = 42 \text{ ns}$$

$$\frac{16}{1.6 \text{ GHz}} = 10 \text{ ns}$$



code opt



Remove instrs

More efficient implementation
fewer clock cycles for same work
Arch improvements, Memory system etc.

grows over time/
then flattened out

grows over time/
then flattened out

DMIPS

f_{clock}

Removes clock scaling impact

3/23/21A

(Min)

CMP R0, R1 → Z, N, V, C

BLT .Lsmaller if R0 < R1

MOV R2, R1

B .Lend

.Lsmaller: MOV R2, R0

.Lend: ~~~~~

CMP
BLT

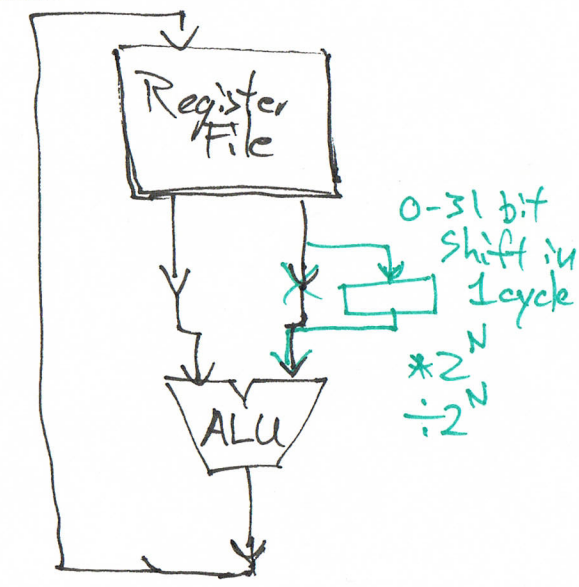
MOV B

.Lend

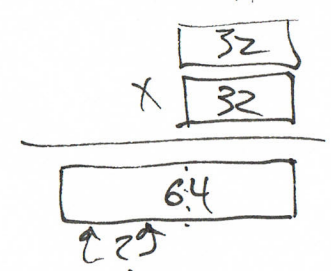
address doesn't increment as usual
→ pipeline stall

CMP R0, R1
MOVGE R2, R1 X
MOVL T R2, R0

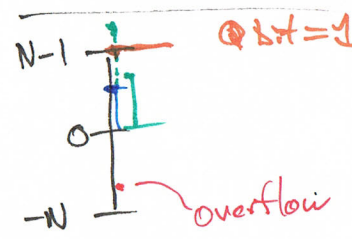
Barrel Shifter



Multiply



Saturated Math



Bit Field

