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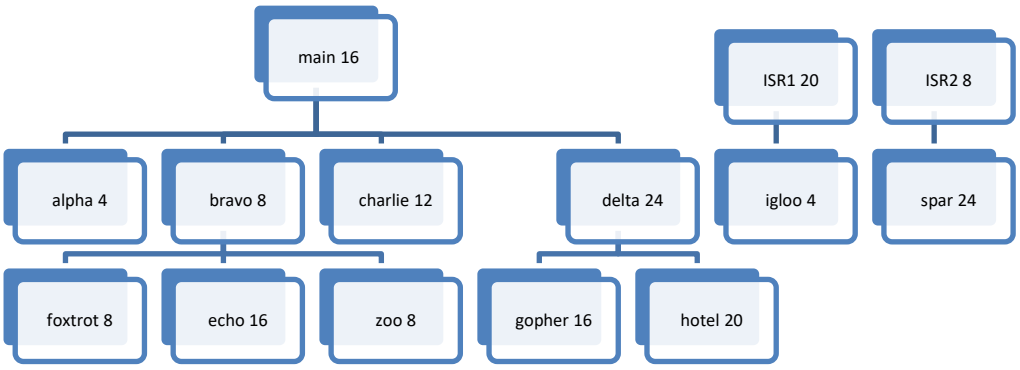
ECE 461/561, Spring 2022: Quiz 3: SOLUTIONS

Analyzing and "Optimizing" for Memory Size, Power or Energy

Memory Size

This diagram shows the maximum stack memory use in bytes for each function and two interrupt handlers in a **single-threaded** program.



1. [10] What is the sequence of function calls (ignoring interrupts) which causes the maximum stack depth, and what is that stack depth?

   main – delta – hotel.
   60 bytes

2. Consider the maximum possible stack depth including interrupts, assuming interrupt handlers are not interruptable.
   a. [8] Fill in the table below to show the call stack: label the items on the stack (e.g. "foo" stack frame) and their sizes. State any other assumptions for full credit.

Description	RAM Used (Bytes)
spar stack frame	24
ISR2 stack frame	8
hardware-stacked register context	32
hotel stack frame	20
delta stack frame	24
main stack frame	16

   b. [2] What is the maximum stack depth in bytes?

      2 pts: 124 bytes total

3. [5+5] What are the two main methods for estimating stack depth? What is the main drawback for each?
   Analytical estimation uses a **function call graph to determine function nesting and then combine per-function stack use** to determine the **maximum possible stack depth per thread or handler**. Then each thread's depth is augmented with the deepest possible handler/ISR activity.
   It typically **over-estimates the maximum stack depth** because it requires more sophisticated analysis to **rule out impossible cases**.

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Experimental estimation involves measuring the amount of stack space used (e.g. with high water marking) as the program runs through many different test cases. It typically **under-estimates the maximum stack depth** because it depends on getting just the right data and timing to **trigger the worst-case behavior**.

4. [5+5] What are the two main reasons that passing more than four parameters to a function increases code size?
   At most four parameters can be passed by register. Other parameters must be passed on the stack.
   Before calling the subroutine function, we need instructions to copy (Mem-Reg-Mem) or push (R-M) arguments onto stack.
   Within the called subroutine function, we need instructions to read the arguments off the stack into registers (M-R) before processing them.

5. [10] Consider the following source code fragment which defines several static (not automatic) variables. Determine the amount of ROM and RAM used by each variable. Assume the compiler does not pack data structures or compress initialization data.

```
int LCD_timeout_counter = LCD_TIMEOUT_COUNT_START;
uint8_t LCD_TS_Calibrated = 1;
const uint32_t LCD_TS_X_Scale=209;
```

Variable	ROM Used (Bytes)	RAM Used (Bytes)
LCD_timeout_counter	4	4
LCD_TS_Calibrated	1	1
LCD_TS_X_Scale	4	0

6. [10] **ECE 561 Only:** Under what conditions does function in-lining reduce **both** code size and execution time?
   Compare code B of function body with code PPE for preparing parameters (in calling function), and prolog/epilog (in called function). Overall execution time will be reduced by any inlining. Overall code size will be reduced if total ROM space taken by all inlined copies of B is smaller than PPE.

Power and Energy

7. [10] Complete the table to indicate whether the types of power depend on the given parameters.

	Depends on supply voltage?	Depends on frequency?
Static power	yes	no
Dynamic power	yes	yes

8. [10] **ECE 561 Only:** Assume an MCU draws 3.8 mA at 3.3 V. It is powered by a linear voltage regulator with an input voltage of 6.0 V and a quiescent current of 5 mA.
   a. [5] How much power does the MCU use?
      MCU uses 3.3 V * 3.8 mA = 12.54 mW

   b. [5] How much power does the regulator use?

      Regulator power use: drop MCU current from input to output voltage + quiescent power

      (6.0 V – 3.3 V) * 3.8 mA + 6.0 V * 5 mA = 10.26 mW + 30 mW = 40.26 mW

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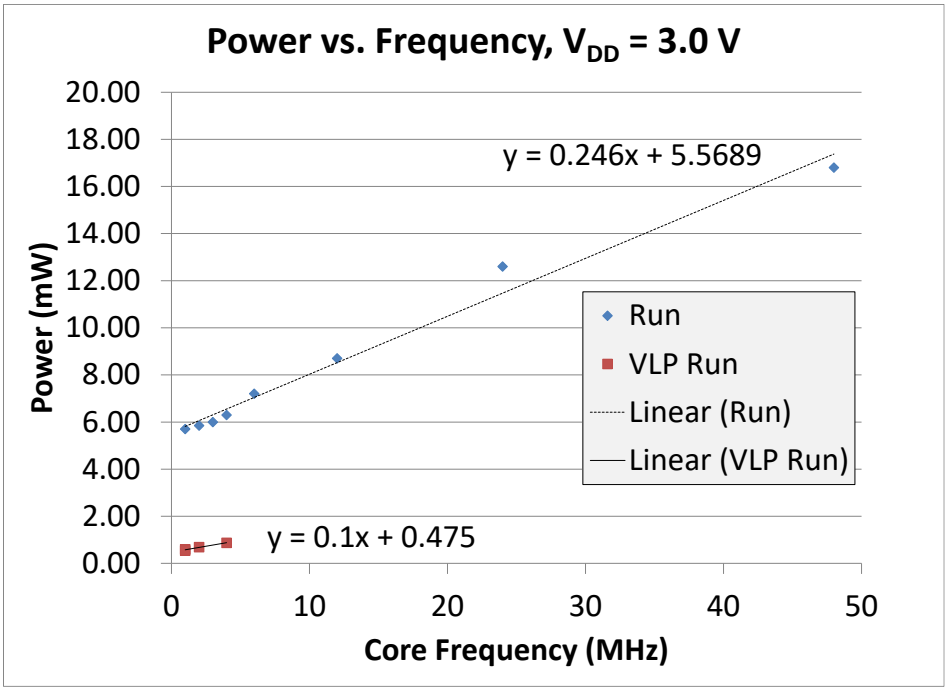
Selected power vs. MCU core frequency characteristics of the KL25Z128 MCU are shown below.



9. Consider the MCU operating at 46 MHz in Run mode at 2.0 V.
   a. [5] What is the power consumption?

$$P = \frac{2.0\ V}{3.0\ V}\left(46\ MHz * 0.246\frac{mW}{MHz} + 5.5689\ mW\right) = 11.257\ mW$$

   b. [5] How much energy is used per clock cycle?

$$E = \frac{11.257\ mW}{46\ MHz} = 244.7\ pJ$$

10. Consider the MCU operating at 3.5 MHz in VLP Run mode at 2.5 V.
   a. [5] What is the power consumption?

$$P = \frac{2.5\ V}{3.0\ V}\left(3.5\ MHz * 0.1\frac{mW}{MHz} + 0.475\ mW\right) = 0.833 * 0.825\ mW = 0.6875\ mW$$

   b. [5] How much energy is used per clock cycle?

$$Energy = \frac{0.6875\ mW}{3.5\ MHz} = 196.4\ pJ$$